

# ZXEvolution rev.C

## TOP SIDE

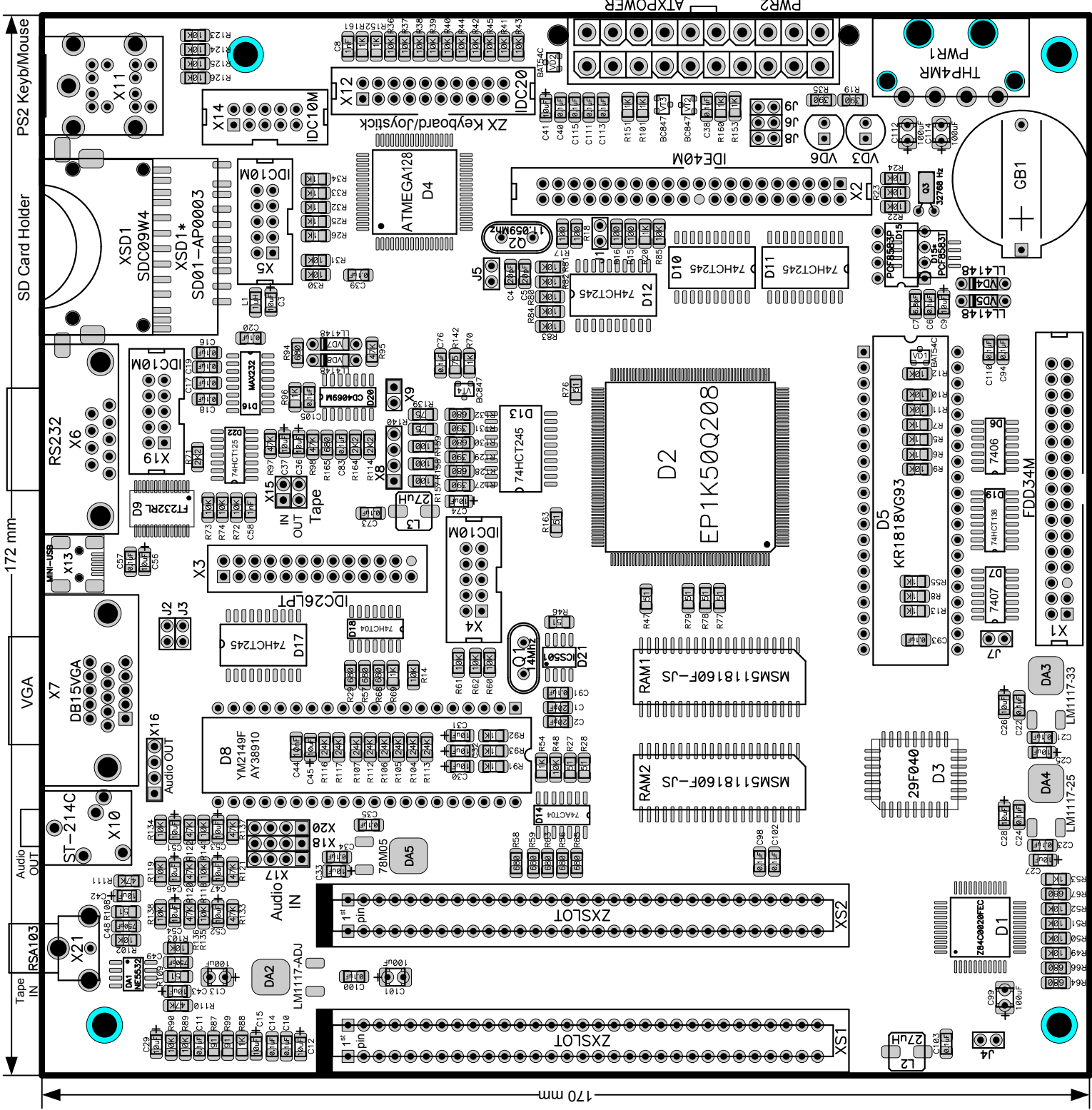
Version: 8 April 2012

### JUMPERS

- J1 – Enable IDE hard reset;
- J2 – Enable composite sync to VGA;
- J3 – Enable +5V to VGA;
- J4 – Enable +12V to ZXBUS slots;
- J5 – Enable external clock to ATMEGA;
- J6 – Soft reset button;
- J7 – Enable HLT to IP on FDC1793;
- J8 – NMI button;
- J9 – Hard reset button.

### CONNECTORS FOR DOWNLOAD FIRMWARE

- X5 – FPGA JTAG for EP1K50QC208. Compatible with ByteBlasterMV (Altera specification).
- X4 – AVR ISP for ATmega128. Compatible with ByteBlasterMV (Altera specification).
- X14 – AVR JTAG for ATmega128. Compatible with AVR JTAG ICE (Atmel specification).



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BOTTOM SIDE

